



Wafer Level 3-D ICs Process Technology (Integrated Circuits and Systems)

From Springer



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This book focuses on foundry-based process technology that enables the fabrication of 3-D ICs. The core of the book discusses the technology platform for pre-packaging wafer level 3-D ICs. However, this book does not include a detailed discussion of 3-D ICs design and 3-D packaging. This is an edited book based on chapters contributed by various experts in the field of wafer-level 3-D ICs process technology. They are from academia, research labs and industry.

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Bibliography

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Editorial Review

From the Back Cover

Wafer Level 3-D ICs Process Technology focuses on foundry-based process technology that enables the fabrication of 3-D ICs. The core of the book discusses alternative technology platforms for pre-packaging wafer level 3-D ICs, with an emphasis on wafer-to-wafer stacking. Driven by the need for improved performance, a number of companies, consortia and universities are researching methods to use short, monolithically-fabricated, vertical interconnections to replace the long interconnects found in 2-D ICs. Stacking disparate technologies to provide various combinations of densely-packed functions, such as logic, memory, MEMS, displays, RF, mixed-signal, sensors, and power delivery is potentially possible with 3-D heterogeneous integration, making this technology the "Holy Grail" of system integration.

Wafer Level 3-D ICs Process Technology is an edited book based on chapters contributed by various experts in the fields of wafer-level 3-D ICs process technology and applications enabled by 3-D integration.

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