



## Network Processor Design: Issues and Practices (The Morgan Kaufmann Series in Computer Architecture and Design)

By Mark A. Franklin, Patrick Crowley, Haldun Hadimioglu, Peter Z. Onufryk



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As the demand for digital communication networks has increased, so have the challenges in network component design. To meet ever-escalating performance, flexibility, and economy requirements, the networking industry has opted to build products around network processors. These new chips range from task-specific processors, such as classification and encryption engines, to more general-purpose packet or communications processors. Programmable yet application-specific, their designs are tailored to efficiently implement communications applications such as routing, protocol analysis, voice and data convergence, firewalls, VPNs, and QoS.

Network processor design is an emerging field with issues and opportunities both numerous and formidable. To help meet this challenge, the editors of this volume created the first Workshop on Network Processors, a forum for scientists and engineers from academia and industry to discuss their latest research in the architecture, design, programming, and use of these devices. In addition to including the results of the Workshop in this volume, the editors also present specially commissioned material from practicing designers, who discuss their companies' latest network processors. *Network Processor Design: Issues and Practices* is an essential reference on network processors for graduate students, researchers, and practicing designers.

\* Includes contributions from major academic and industrial research labs including Aachen University of Technology; Cisco Systems; Infineon Technologies; Intel Corp.; North Carolina State University; Swiss Federal Institute of Technology; University of California, Berkeley; University of Dortmund; University of Washington; and Washington University.

\* Examines the latest network processors from Agere Systems, Cisco, IBM, Intel, Motorola, Sierra Inc., and TranSwitch.

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## Editorial Review

Review

*"Highly recommended for practitioner and researcher alike, Network Processor Design introduces an important group of commercial and proprietary network processors and covers the latest thinking in the design and use of this important new class of application-specific processors."*

--John F. Wakerly, Consulting Professor, Stanford University

From the Back Cover

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## Features

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Washington; and Washington University.

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#### About the Author

**Mark A. Franklin** received his B.A., B.S.E.E. and M.S.E.E. from Columbia University, and his Ph.D. in EE from Carnegie-Mellon University. He is currently at Washington University in St. Louis where he has a joint appointment in Electrical Engineering and Computer Science, and holds the Urbauer Chair in Engineering. He founded and is Director of the Computer and Communications Research Center and until recently was the Director of the Undergraduate Program in Computer Engineering. Dr. Franklin is engaged in research, teaching and consulting in the areas of computer and communications architectures, ASIC and embedded processor design, parallel and distributed systems, and systems performance evaluation. He is a Fellow of the IEEE, a member of the ACM, and has been an organizer and reviewer for numerous professional conferences including the HPCA8 Workshop on Network Processors (2002). He has been Chair of the IEEE TCCA (Technical Committee on Computer Architecture), and Vice-Chairman of the ACM SIGARCH (Special Interest Group on Computer Architecture).

**Patrick Crowley** is an associate Professor in the Department of Computer Science & Engineering at Washington University in St. Louis, Missouri. His research interests are in computer and network systems architecture, with a current focus on the design of programmable embedded network systems and the invention of superior network monitoring and security techniques. He co-founded the ACM/IEEE Symposium on Architectures for Networking and Communications Systems, and co-edited the three-book series, Network Processor Design. He serves as Associate Editor of the IEEE/ACM Transactions on Networking. In 2007, Crowley was chosen to join the DARPA Computer Science Study Group.

**Haldun Hadimioglu** received his BS and MS degrees in Electrical Engineering at Middle East Technical University, Ankara Turkey and his Ph.D. in Computer Science from Polytechnic University in New York. He is currently an Industry Associate Professor in the Computer Science Department and a member of the Computer Engineering faculty at the Polytechnic University. He worked as a research engineer at PETAS, Ankara Turkey (1980-1982). Dr. Hadimioglu's research and teaching interests include Computer Architecture, Parallel and Distributed Systems, Networking and VLSI Design. He was a guest editor of the special issue on "Advances in High Performance Memory Systems," IEEE Transactions on Computers (Nov 2001) and has reviewed papers for leading journals such as the IEEE Transactions on Computers. Hadimioglu is a member of the IEEE, the ACM, and Sigma Xi. He has been an organizer of various workshops including, the ISCA Memory Wall (2000), ISCA Memory Performance Issues (2002, 2001) and HPCA8 Workshop on Network Processors (2002). He received Dedicated Faculty and Outstanding Faculty awards from Polytechnic students in 1995 and 1993, respectively.

**Peter Z. Onufryk** received his B.S.E.E. from Rutgers University, M.S.E.E. from Purdue University, and Ph.D. in Electrical and Computer Engineering from Rutgers University. He is currently a director in the Internetworking Products Division at Integrated Device Technology, Inc. where he is responsible for architecture definition and validation of communications products. Before joining IDT, Peter was a researcher for thirteen years at AT&T Labs - Research (formally AT&T Bell Labs) where he worked on communications systems and parallel computer architectures. These included a number of parallel, cache-coherent multiprocessor and dataflow based machines that were targeted towards high performance military systems. Other work there focused on packet telephony and early network processors. Onufryk is a member

of the IEEE. He was an organizer and program committee member of the HPCA8 Workshop on Network Processors 2002. Peter was the architect of four communications processors as well as numerous ASICs, boards, and systems.

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